Ultra320 SCSI Meets The Challenges.(Technology Information)

Computer Technology Review, June, 2001, by Mark Evans

Improvements in recording technologies continue to increase the rate at which data storage devices can read data from their media and host adapters increase their data transfer capabilities. Standardized definitions for new SCSI transfer rates must be devised to prevent the interface from becoming a performance bottleneck for systems. The ANSI NCITS T10 Technical Committee (often called, "the ANSI SCSI committee" or simply "T10") with input from the SCSI Trade Association (STA) develops standards that define the requirements for the parallel SCSI interface.

Ultra320 SCSI, with a maximum transfer rate of 320MB/sec, is the latest development for the SCSI parallel interface. Additional new features to enhance performance, improve data reliability, and increase ease of use have also been developed by T10. This article will describe the mandatory and optional features defined for Ultra320 SCSI devices. Additional details about these features are available in the ANSI draft standard document SCSI Parallel Interface-4 (SPI-4). The latest revision of this draft is available for review at http://www.t10.org/.

Mandatory Features

DT (Double-transition) data transfers: For "single-transition" (ST) transfers, the maximum frequency of the clock signals is twice the maximum frequency of the data signals because data is only transferred on one edge of the clock. DT transfers provide a method for the ACK and REQ clock signals to have the same maximum frequency as the data signals by using both asserting and negating transitions of ACK and REQ for clocking data. Each transition of the DT clock signal transfers two bytes of data as DT transfers can only be used with wide (16-bit) buses.

Free-running clock (FRC): A free-running clock is used to improve integrity of the clock signal by removing inter-symbol interference (ISI). ISI is the effect that a transition on a signal line has on transitions immediately before or after it on the same line. A pulse (or symbol) will cause a nearby preceding pulse to shift forward in time, and it will cause a nearby subsequent pulse to shift backward in time (i.e., a pulse will "interfere" with the placement in time of its adjacent pulses). By having a clock running at a constant frequency and a separate lower-speed signal for qualification of data, the ISI effect is neutralized. The free-running clock is restricted for use with DT information unit transfers at 320MB/sec.

o

Training pattern: The training pattern is a pre-determined pattern that is transmitted from the sender to the receiver at a specified time. The receiver can use portions of this pattern to perform skew compensation because it knows what the pattern will be (i.e., exactly when data transitions should occur). Other portions of this pattern may be used to perform other signal adjustments such as tuning adaptive active filtering (AAF). The training pattern may be sent before each data transmission or after some period of time or an event such as a bus reset.

Skew compensation of data signals relative to the clock signal: Skew is the difference in time from when one transition launched by a sender arrives at a given point (e.g., a recipient's connector) to when a second transition launched by the sender arrives at the same point. The arrival time difference is caused by several factors including differences in length and electrical characteristics of the two signal paths. If a data transition is skewed so much relative to the clock that it falls outside of the qualifying clock window, the device will not accurately detect data. One of the largest losses in the error budget for Ultra320 SCSI is skew. With the training pattern specified, an Ultra320 SCSI device can establish skew compensation simultaneously for each of the received transitions on the data lines so that they occur at the correct time relative to the clock. Once established, this compensation is used for all subsequent transfers until the next training pattern sequence is initiated.

1 · 2 · 3 · 4 | Next »

RELATED TERMS

- Computer storage devices Standards
- Computer peripherals industry Standards